Amendments to the Claims:

This listing of claims will replace all prior version, and listings, of claims in the application:

Listing of Claims:

Claims 1-7. (CANCELLED)

8. (CURRENTLY AMENDED) An interface for a monitor and a temperature probe including a temperature sensor comprising:

a logic circuit for determining a modified resistive output for the temperature sensor and

a means for providing the modified resistive output, wherein the means for providing the modified resistive output is compatible with the monitor such that the monitor can display a temperature that corresponds to the modified resistive output from the temperature probe, said means including a FET coupled to said logic circuit via a first terminal and via a feedback arrangement, said means providing a FET resistance corresponding to the modified resistive output.

9. (ORIGINAL) The interface of claim 8 wherein the logic circuit is programmed to execute a predictive or a correlative algorithm.

10. (ORIGINAL) The interface of claim 9 wherein the logic circuit is a microprocessor.

Claims 11 – 15. (CANCELLED)

16. (PREVIOUSLY PRESENTED) A temperature probe comprising:

a temperature sensor having a resistive output,

a processor for determining a modified resistive output for the temperature sensor, the processor being programmed to execute a predictive or a correlative algorithm, and

a FET for providing the modified resistive output in response to a signal from the processor,

wherein the algorithm is a predictive algorithm that converts the resistive output of the temperature sensor during a thermally unstable condition to a modified resistive output representative of a predicted temperature during a condition of thermal stability.

17. (ORIGINAL) The temperature probe of claim 16 wherein the processor executes an algorithm to convert the resistive output of the temperature sensor to a modified resistive output that can be displayed by a monitor.

18. (CANCELLED)

19. (PREVIOUSLY PRESENTED) The temperature probe of claim 16 wherein the probe includes two FETs.

Claims 20 -24 (CANCELLED)

25. (PREVIOUSLY PRESENTED) A method for digitally modifying the resistive output of a temperature sensor which comprises inputting the resistive output from the temperature sensor to a logic circuit, implementing a predictive or a

correlative algorithm using the logic circuit to determine a modified resistive output, controlling a gate of a FET to adopt a setting corresponding to the modified resistive output, and outputting a resistance corresponding to the modified resistive output.

26. (CANCELLED)

27. (PREVIOUSLY PRESENTED) A temperature probe comprising:

a temperature sensor that provides a resistive output,

a logic circuit for determining a modified resistive output for the temperature sensor, and

a means for providing the modified resistive output including a FET,

wherein the logic circuit is a microprocessor programmed to execute a predictive or a correlative algorithm, and

wherein the microprocessor includes an output and the FET includes a gate, where the output of the microprocessor controls the gate of the FET such that the FET provides a FET resistance corresponding to the modified resistive output.

28. (PREVIOUSLY PRESENTED) The temperature probe of claim 27 wherein the microprocessor further includes:

a first input from a first amplifier, where the first amplifier measures a FET voltage of the FET, and

a second input from a second amplifier, where the second amplifier measures a resistor voltage of a resistor having a first resistance,

where the microprocessor calculates a FET current using the first resistance and the resistor voltage from the second input, calculates a FET resistance using the FET voltage from the first input and the FET current, compares the FET resistance to the modified resistive output and applies a difference between the FET resistance and the modified resistive output as a negative feedback to the gate.

29. (CANCELLED)

30. (PREVIOUSLY PRESENTED) An interface for a monitor and a temperature probe including a temperature sensor comprising:

a logic circuit for determining a modified resistive output for the temperature sensor and

a means for providing the modified resistive output, wherein the means for providing the modified resistive output includes a FET, and

wherein the logic circuit includes an output and the FET includes a gate, where the output of the logic circuit controls the gate of the FET such that the FET provides a FET resistance corresponding to the modified resistive output.

31. (PREVIOUSLY PRESENTED) The interface of claim 30 wherein the logic circuit further includes:

a second input from a second amplifier, where the second amplifier measures a resistor voltage of a resistor having a first resistance,

where the logic circuit calculates a FET current using the first resistance and the resistor voltage from the second input, calculates a FET resistance using the FET voltage from the from the first input and the FET current, compares the FET resistance to the modified resistive output and applies a difference between

the FET resistance and the modified resistive output as a negative feedback to the gate.

32. (PREVIOUSLY PRESENTED) A temperature probe comprising:

a temperature sensor having a resistive output,

a processor for determining a modified resistive output for the temperature sensor, the processor being programmed to execute a predictive or a correlative algorithm, and

a FET for providing the modified resistive output in response to a signal from the processor,

wherein the processor includes an output and the FET includes a gate, where the output of the processor controls the gate of the FET such that the FET provides a FET resistance corresponding to the modified resistive output.

33. (PREVIOUSLY PRESENTED) The temperature probe of claim 32 wherein the processor further includes:

a first input from a first amplifier, where the first amplifier measure a FET voltage of the FET, and

a second input from a second amplifier, where the second amplifier measures a resistor voltage of a resistor having a first resistance,

where the processor calculates a FET current using the first resistance and the resistor voltage from the second input, calculates a FET resistance using the FET voltage from the first input and the FET current, compares the FET resistance to the modified resistive output and applies a difference between the FET resistance and the modified resistive output as a negative feedback to the gate.

34. (PREVIOUSLY PRESENTED) The method of claim 25 further including measuring a FET voltage with a first amplifier, measuring a resistor voltage of a first resistor having a first resistance, calculating a FET current using the first resistance and the resistor voltage, calculating a FET resistance using the FET voltage and the FET current, comparing the FET resistance to the modified resistive output and applying a difference between the FET resistance and the modified resistive output as a negative feedback to the gate.

Claims 35 – 40. (CANCELLED)